In the specification:

Please replace the paragraph beginning at page 11, line 7 with the following rewritten paragraph:

-- Referring to Figure 9, a second etch step, which is anisotropic, is carried out to remove substantially all of the horizontally-exposed portions of sleeve insulator layer 50 from the bottom of the partially formed BLCC. Sleeve insulator layer 50 thus covers the exposed portions of capacitor cell dielectric layer 44, cell plate layer 46, and cell plate insulating layer 48 that are within contact hole 70. As illustrated in Figure 9, sleeve insulator layer 50 thus has a first terminus substantially adjacent to cell plate insulating layer 48. Sleeve insulator layer 50 also has a second terminus opposite the first terminus, the second terminus being located below capacitor cell dielectric layer 44 and between the upper and lower surfaces of, or within, lower bulk insulator layer 36.--

D1

Please replace the paragraph beginning at page 14, line 17 with the following rewritten paragraph:

~~Referring to Figure 14, a circle 80 illustrates in phantom a cross-section of an etch hole through upper bulk insulator layer 51. A center line 80 represents an axis passing through the center of circle 80. In Figure 14, center line 71 represents the axis passing through the center of sleeve insulator layer 50. The symbol Δ_3 represent the misalignment from the center of circle 80 to the center of sleeve insulator layer 50. As with sleeve insulator layer 50 in Figure 9, sleeve insulator layer 50 in Figure 14 has a first terminus substantially adjacent to cell plate insulating layer 48. Sleeve insulator layer 50 also has a second terminus opposite the first terminus, the second terminus being located below capacitor cell dielectric layer 44 and between the upper and lower surfaces of, or within, lower bulk insulator layer 36.~~

D2

Please replace the paragraph beginning at page 15, line 15 with the following rewritten paragraph:

The process creating the structure seen in Figure 14 is substantially the same as that creating the structure seen in Figure 15. In Figure 15, a circle 90 illustrates in phantom a cross-section of an etch hole through upper bulk insulator layer 51. The etch hole is aligned with respect to sleeve insulator layer 50. As with sleeve insulator layer 50 in Figure 9, sleeve insulator layer 50 in Figure 15 has a first terminus substantially adjacent to cell plate insulating layer 48. Sleeve insulator layer 50 also has a second terminus opposite the first terminus, the second terminus being located below capacitor cell dielectric layer 44 and between the upper and lower surfaces of, or within, lower bulk insulator layer 36. Also, the etch is self aligned with sleeve insulator layer 50 due to the selectivity of the etch with respect to the material from which sleeve insulator layer 50 is substantially composed, and due to the etch selectivity to the material of which cell plate insulating layer 48 is composed. As was described with respect to Figure 13, the self-alignment of the etch through sleeve insulator layer 50 in effect assures electrical insulation of cell plate layer 46 to prevent an electrical short with electrically conductive bit line contact 92 within the BLCC. Figure 15 illustrates the maximum contact size on active area 18b, as dictated by the diameter of the area defined within sleeve insulator layer 50. Electrical insulation protection of bit line contact 92 is provided by cell plate insulating layer 48 and sleeve insulator layer 50 so as to prevent shorting of cell plate layer 46 with bit line contact 92.

D3

Please replace the paragraph beginning at page 16, line 3 with the following rewritten paragraphs:

Figure 16 shows the divergent types of contacts that can be made using the invention, although all of the depicted contacts need not be present in the same structure nor be situated as depicted in Figure 16. In Figure 16, circle 90 illustrates in phantom a cross-section of an etch hole, made by conventional etch processes, through upper bulk insulator layer 51. A contact plug 72 in upon source/drain region 18b. Electrically conductive bit line contact 92 is situated within contact hole 70 and passes through sleeve insulator layer to terminate upon contact plug 72. As with sleeve insulator layer 50 in Figure 9, sleeve insulator layer 50 in Figure 16 has a first terminus substantially adjacent to cell plate insulating layer 48. Sleeve insulator layer 50 also has a second terminus opposite the first terminus, the second terminus being located below capacitor cell dielectric layer 44 and between the upper and lower surfaces of, or within, lower bulk insulator layer 36.

Circle 94 illustrates in phantom a cross-section of a contact hole 98, made by conventional etch processes, through upper bulk insulator layer 51 and into a transistor stop on a gate 24 beneath an insulating protective layer 28 of a transistor. Electrically conductive contact 100 is situated within contact hole 98 and passes through a sleeve insulator layer 52 to make contact with gate 24. Sleeve insulator layer 52 in Figure 16 has a first terminus substantially adjacent to cell plate insulating layer 48. Sleeve insulator layer 52 also has a second terminus opposite the first terminus, the second terminus being located below capacitor cell dielectric layer 44, between the upper and lower surfaces of, or within, lower bulk insulator layer 36, and in contact with storage node layer 42.

Circle 104 illustrates in phantom a cross-section of a contact hole 106, made by conventional etch processes, through upper bulk insulator layer 51 and into storage node layer 42. Electrically conductive contact 102 is situated within contact hole 106 and passes through a sleeve insulator layer 53 to make contact with storage node layer 42. Sleeve insulator layer 53 insulates electrically

conductive contact 102 from cell plate layer 46. Sleeve insulator layer 53 in Figure 16 has a first terminus substantially adjacent to cell plate insulating layer 48. Sleeve insulator layer 53 also has a second terminus opposite the first terminus, the second terminus being located below capacitor cell dielectric layer 44 and in contact with storage node layer 42.

D4